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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,764	11/25/2003	Masashi Yonemaru	829-618	3114

23117 7590 01/27/2006

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,764	YONEMARU, MASASHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,7 and 9-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/27/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by OOISHI ET AL. (2002/0057111).

Ooishi et al. discloses a semiconductor integrated circuit, comprising a first cell (Note that Ooishi et al. refer to their cells as "stages") comprising a plurality of transistors 41,42 including a PMOS transistor 41 and an NMOS transistor 42; and a

second cell comprising a PMOS transistor section 53-54, the PMOS transistor section 53-54 comprising a first PMOS transistor 53 and a second PMOS transistor 54 connected to the first PMOS transistor 53 in series, and an NMOS transistor section 55-56, the NMOS transistor section 55-56 comprising a first NMOS transistor 56 and a second NMOS transistor 55 connected to the first NMOS transistor 56 in series, wherein a predetermined scheme is used to connect between the first cell and the second cell, between the plurality of transistors 41,42 in the first cell, and between the PMOS transistor section 53-54 and the NMOS transistor section 55-56 in the second cell, wherein the first cell functions as a logic operation (note paragraph 0039, stating "data are transferred [i.e. output] from the latch portion of former stage [cell 1] to the latch portion of latter stage.") circuit for outputting data; and the second cell functions as a driver circuit for driving (via feedback signal TG2B) the logic operation circuit and a data retaining circuit (the flip-flop circuit seen in figure 2) for retaining data output by the logic operation circuit, and wherein the first PMOS transistor 53, the second PMOS transistor 54, the first NMOS transistor 56, and the second NMOS transistor 55 each comprise a gate, a source, and a drain (gates, sources and drains are understood to be present in the transistors presented diagrammatically in figure 2); a first source voltage VCC1 is applied to the source of the first PMOS transistor 53; a second source voltage (GND) is applied to the source of the first NMOS transistor 56; the gate of the second PMOS transistor 54 is connected to an input terminal, an input signal (output from latch 51-52 being input to the input terminal), and the gate of the (other PMOS transistor) first

PMOS transistor 53 is connected to a first gate control signal input terminal (being the terminal to which first gate control signal TG2 is applied), a first gate control signal TG2 being input to the first gate control signal input terminal; the gate of the second NMOS transistor 55 is connected to the input terminal (that is, the terminal to which output from latch 51-52 is input), and the gate of the first NMOS (the other NMOS) transistor 56 is connected to a second gate control signal input terminal (TB2B signal terminal), a second (TB2B) gate control signal being input to the second gate control signal input terminal; and the drain of the second PMOS transistor 54 and the drain of the second NMOS transistor 55 are connected to an output terminal Q (through output processors 57-58). Note figure 2 and paragraphs 0033-0043 of Ooishi et al.

Response to Arguments

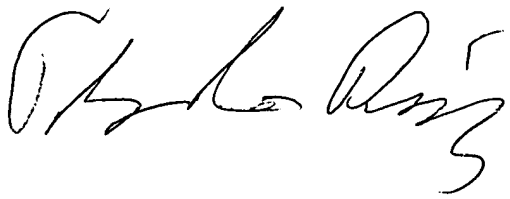
3. Applicant's arguments with respect to claims 1, 6, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
01/06